VL725 CMOS NANOTECHNOLOGY 3-0-0 -3

Brief History of Semiconductor technology, CMOS Scaling Trends and Scaling Methodologies, ITRS Roadmap; Overview of silicon process technology - crystal growth, gate dielectrics, Photolithography, Implantation, Deposition, Etching; Interconnect Technology, Copper Dual Damascene process, Silicon photonics; Silicides, Shallow and Deep Trench Isolation, CMOS Process flow, Nanoscale CMOS Gate dielectrics and gate electrodes for sub-100nm technology, Low K Dielectrics, Strained silicon, Silicon Germanium, Techniques to overcome Short Channel Effects, Nanolithography techniques, SOI Technology, Ultra Shallow Junction. Multiple Gate MOSFETs – Fin FETs.

TEXTBOOKS/ REFERENCES:

1. Marc J. Madou, "Fundamentals of Microfabrication and Nanotechnology -Volume II", 3rd Edition, CRC Press, 2011.
2. Peter Van Zant, "Microchip Fabrication: A Practical Guide to Semiconductor Processing", 6th Edition, McGraw-Hill Professional, 2014.
3. Howard Huff, "Into the Nano Era: Beyond Planar Silicon CMOS", Springer, 2009.
4. Stanley Wolf, "Silicon Processing for VLSI Era", Vol. 4, Lattice Press, 2002.
5. Stephen Campbell, "Science of Microelectronic Fabrication", Oxford University Press, 2001.
6. James D. Plummer, Michael D. Deal, Peter B. Griffin, "Silicon VLSI Technology: Fundamentals, Practice and Modeling", Prentice Hall India Private Limited, 2000.