M.TECH - VLSI DESIGN

Department of Electronics and Communication Engineering

Very Large Scale Integrated (VLSI) Circuit Design is the process of designing a large computer chip (more specifically, an integrated circuit, or IC), using computer-aided design (CAD) tools on a workstation or a personal computer (PC).

The course demands learning the principles of VLSI design, designing and fabricating the state-of-the-art VLSI chips, understanding the complete design flow and expertise to design CMOS chips for industrial requirements. The curriculum focuses on employing hierarchical design methods and understanding the design issues at the various levels of hierarchy. Students are exposed to various design softwares in this programme. Also, they learn to design, simulate, implement and test complex digital systems using FPGAs (Field Programmable Gate Arrays). The main objectives of this course are to analyze the electrical and design characteristics of transistors, gates and to study the issues and methodologies involved in the integration of these devices into complex high-performance systems.

CURRICULUM

First Semester

Course Code	Type	Course	L	T	P	Cr
MA601	FC	Linear Algebra, Probability and Graph Theory	3	1	0	4
VL602	FC	Semiconductor Device Physics	3	0	0	3
VL611	SC	CMOS Digital Integrated Circuits	3	0	0	3
VL612	SC	Digital Design	3	0	0	3
VL613	SC	Analysis and Design of Analog Integrated Circuits	3	0	1	4
VL614	SC	VLSI Design Lab I	0	0	1	1
HU601		Cultural Education*				P/F
					Credits	**18**

*Non Credit course

Second Semester

Course Code	Type	Course	L	T	P	Cr
VL615	SC	CMOS Digital Sub-system Design	3	0	1	4
VL616	SC	Low Power VLSI Circuits	3	0	0	3
VL617	SC	Testing of VLSI Circuits	3	0	0	3
	E	Elective I	3	0	0	3
	E	Elective II	3	0	0	3
VL618	SC	Seminar	0	0	2	2
VL619	SC	VLSI Design Lab II	0	0	2	2
EN600		Technical Writing*				P/F
					Credits	**20**

*Non Credit course

Third Semester

Course Code	Type	Course	L	T	P	Cr
	E	Elective III	3	0	0	3
	E	Elective IV	3	0	0	3
VL799	P	Dissertation				8
					Credits	**14**

Fourth Semester

Course Code	Type	Course	L	T	P	Cr
VL799	P	Dissertation				14
					Credits	**14**
					Total Credits	**66**

List of Courses

Foundation Core

Course Code	Course	L	T	P	Cr
MA601	Linear Algebra, Probability and Graph Theory	3	1	0	4
VL602	Semiconductor Device Physics	3	0	0	3

Subject Core

Course Code	Course	L	T	P	Cr
VL611	CMOS Digital Integrated Circuits	3	0	0	3
VL612	Digital Design	3	0	0	3
VL613	Analysis and Design of Analog Integrated Circuits	3	0	1	4
VL614	VLSI Design Lab I	0	0	1	1
VL615	CMOS Digital Sub-system Design	3	0	1	4
VL616	Low Power VLSI Circuits	3	0	0	3
VL617	Testing of VLSI Circuits	3	0	0	3
VL618	Seminar	0	0	2	2
VL619	VLSI Design Lab II	0	0	2	2

Electives

Course Code	Course	L	T	P	Cr
VL701	Digital Signal Processing	3	0	0	3
VL702	Embedded Systems	3	0	0	3
VL703	CMOS RF System Design	3	0	0	3
VL704	Nano Electronics	3	0	0	3
VL705	VLSI Signal Conditioning	3	0	0	3
VL706	System on Chip Design	3	0	0	3
VL707	VLSI Architectures for Multi-Core and Heterogeneous Computing	3	0	0	3
VL708	Analog Sub-system Design	3	0	0	3
VL709	VLSI Signal Processing	3	0	0	3
VL710	Hardware Software Co-design	3	0	0	3
VL711	VLSI Hardware Security and Trust	3	0	0	3
VL712	Reconfigurable Computing	3	0	0	3
VL713	Electronic System Level Design	3	0	0	3

VL714	Monolithic Microwave Integrated Circuits	3	0	0	3
VL715	Design for Test	3	0	0	3
VL716	Network on Chip	3	0	0	3
VL717	Optimization Techniques for VLSI Design	3	0	0	3
VL718	Wavelets and Applications	3	0	0	3
VL719	Semiconductor Memory Design	3	0	0	3
VL720	Static Timing Analysis	3	0	0	3
VL721	Synthesis and Verification of VLSI Logic Design	3	0	0	3
VL722	Optoelectronic Devices	3	0	0	3

Project Work

Course Code	Course	L	T	P	Cr
VL799	Dissertation				8
VL799	Dissertation				14

MA601 LINEAR ALGEBRA, PROBABILITY AND GRAPH THEORY 3-1-0-4

Review of Matrix Algebra – Vector Spaces – Sub Spaces – Linear Independence – Basis – Dimension – Null Space – Rank and Nullity – Inner Product – Orthogonality – Orthogonal Basis – Gram-Schmitt Process – Statistics and Probability – Probability Laws – Addition and Multiplication Theorems on Probability – Baye's Theorem – Expectation – Moments and Moment Generating Function of Discrete and Continuous Distributions – Binomial – Poisson and Normal Distributions – Introduction to Graph Theory – Basic Definitions and Examples – Trees and their Characterization – Euler Circuits – Long Paths and Cycles – Vertex Colourings – Brooks Theorem – Chromatic Polynomial – Edge Colourings – Vizing's Theorem – Planar Graphs – Including Euler's Formula – Dual Graphs.

TEXT BOOKS / REFERENCES:

1. H. Anton and C. Rorres, *Elementary Linear Algebra: Applications Version*, Tenth Edition, Wiley, 2010.
2. D.C. Montgomery and G.C. Runger, *Applied Statistics and Probability for Engineers*, Fourth Edition, John Wiley and Sons, 2006.
3. N. Deo, *Graph Theory with Applications to Engineering and Computer Science*, Prentice Hall India Learning Pvt. Ltd., 2004.
4. E. Kreyszig, *Advanced Engineering Mathematics*, Eighth Edition, John Wiley and Sons, 2010.

VL602 SEMICONDUCTOR DEVICE PHYSICS 3-0-0-3

Review of Semiconductor Structure and Quantum Mechanics – Energy Bands and Charge Carriers in Semiconductors – Doping and Carrier Concentration – Fermi Energy – Drift of Carriers – Transport Equation – Carrier Generation and Recombination – Excess Carriers – Diffusion of Carriers and Recombination – Continuity Equation – Ambi-polar Transport – Gradients in Quasi-Fermi Levels – Haynes-Shockley Experiment – PN Junction at Equilibrium – Forward and Reverse Bias Conditions – Transient and AC Conditions – Breakdown – Capacitance of PN Junctions – Metal-Semiconductor Junctions – The Ideal MOS Capacitor – Effect of Real Surfaces – MOSCAP Characteristics – MOSFET Characteristics – Threshold Voltage – Mobility – Substrate Bias – Sub-threshold Characteristics – MOSFET Scaling and Hot-carrier Effects – Short-channel Effects – Fundamentals of BJT – Amplification – Minority Carrier Distribution – Terminal Currents – Coupled Diode Model – Charge Control Analysis – Non-ideal Effects.

TEXT BOOKS / REFERENCES:

1. D.A. Neamen, *Semiconductor Physics and Devices: Basic Principles*, Third Edition, McGraw-Hill International, 2003.
2. B.G. Streetman and S.K. Banerjee, *Solid State Electronic Devices*, Sixth Edition, Prentice Hall India, 2010.
3. S.M. Sze and K.K. Ng, *Physics of Semiconductor Devices*, Third Edition, John Wiley and Sons Inc., 2007.
4. Y. Taur and T.H. Ning, *Fundamentals of Modern VLSI Devices*, Second Edition, Cambridge University Press, 2009.

VL611 CMOS DIGITAL INTEGRATED CIRCUITS 3-0-0-3

NMOS and PMOS Transistors – Threshold Voltage – Body Effect – Second-order Effects – NMOS and CMOS Inverters – Inverter Ratio – DC and Transient Characteristics – Switching Times – Driving Large Capacitance Loads – CMOS Logic Structures – Transmission Gates – Static CMOS Design – Dynamic CMOS Design – Parasitic Estimation – Switching Characteristics – Transistor Sizing – Power Dissipation and Design Margining – Charge Sharing – Logical Effort – Scaling – Combinational Circuits.

TEXT BOOKS / REFERENCES:

1. J.M. Rabaey, A.P. Chandrakasan and B. Nikoli , *Digital Integrated Circuits: A Design Perspective*, Second Edition, Prentice Hall India, 2003.
2. S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits - Analysis and Design*, Third Edition, Tata McGraw-Hill, 2003.
3. N.H.E. Weste and D.M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Fourth Edition, Addison Wesley, 2010.

VL612 DIGITAL DESIGN 3-0-0-3

Register Files – FIFOs – LIFOs – SIPOs – Bidirectional Shift Register – Universal Shift Register – Barrel Shifter – Linear Feedback Shift Registers – Memory – RAM – Static RAM – Dynamic RAM – Serial Access Memory – ROM – Content Addressable Memory – Booth Multiplier – Wallace Tree Multiplier – Baugh-Wooley Multiplier – Design and Synthesis of Data Path Controller – Introduction to FSM and State Diagram – State Diagram to Control External Hardware Subsystems – Synthesis of Hardware from a State Diagram – Synchronous FSM Design – One-hot Technique in FSM Design – Asynchronous FSM Design – Programmable Logic and Storage – Algorithm and Architecture for Digital Processor Design – Architecture for Arithmetic Processor – Post Synthesis Design.

TEXT BOOKS / REFERENCES:

1. M.D. Ciletti, *Advance Digital Design with Verilog HDL*, Pearson Higher Education, 2011.
2. P.M. and L. Elliott, *FSM based Digital Design using Verilog HDL*, John Wiley and Sons Ltd, 2008.
3. P.K. Lala, *Principles of Modern Digital Design*, John Wiley and Sons Ltd., 2007.

VL613 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS 3-0-1-4

MOS Transistor basic Operation – Large-signal Modeling – Body Effect – Low-frequency Small-signal Modeling – High-frequency Small-signal Modeling – Advanced MOS Modeling – Sub-threshold Operation – Short-channel Effects – Leakage Current – Passive Devices – Resistors – Capacitors – Single-stage Amplifier Topologies – Common Source – Source Follower – Common Gate – Source-degenerated Cascode Current Mirrors – Wide-swing Current Mirrors – Enhanced Output Impedance Current Mirrors – Gain-boosting Current Mirror – Differential Amplifiers – CMRR – Review of Frequency Response of Linear Systems – Miller Theorem and Miller Effect – High-frequency MOS Small-signal Model – Frequency Response of Single-stage Amplifier Topologies – Differential Pair – Feedback – Ideal Model of Negative

Feedback – Dynamic Response of Feedback Amplifiers – Inverting and Non-Inverting Amplifiers – Loop Gain – Two-Stage CMOS Op-amp – Gain and Frequency Response – Slew Rate – Systematic Offset – Frequency Compensation of Two-Stage Op-amps – Dominant Pole Compensation.

TEXT BOOKS / REFERENCES:

1. T.C. Carusone, D.A. Johns and K.W. Martin, *Analog Integrated Circuit Design*, Second Edition, John Wiley Inc, 2012.
2. B. Razavi, *Design of Analog CMOS Integrated Circuits*, Tata McGraw-Hill, 2002, (Reprint 2008).
3. P.E. Allen, and D.R. Holberg, *CMOS Analog Circuit Design*, Third Edition, Oxford Press, 2011.
4. P.R. Gray, P.J. Hurst, S.H. Levis and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley and Sons Inc., 2009.

VL614 VLSI DESIGN LAB I 0-0-1-1

Design – Simulation and Synthesis using Gate level – Dataflow – Behavioral Modeling – Downloading into FPGA – Design and Implementation of Peripheral Controller Chips.

TEXT BOOKS / REFERENCES:

Laboratory Manuals

VL615 CMOS DIGITAL SUB-SYSTEM DESIGN 3-0-1-4

Design Consideration – Digital Processor Structure – Data Path – Bus Architecture – 4-bit Shifter – ALU Subsystem – 4-bit Adder – Bit Serial Adders – Carry Save Adders – Carry Look Ahead Adders – Carry Skip Adders – Parity Generator – Comparators – Zero/one detectors – Binary counters – Boolean operations – Control Logic Implementation – PLA Control Implementation – ROM Control Implementation – Multilevel logic – An Example of Control Logic Implementation – Static Timing Analysis – Static Timing Analysis Concepts – Timing Exceptions – Timing Violations – Timing – Clocks – Input / Output Timing – False Paths – Multi-Cycle Paths – Constraining Internal Register – Register Paths – Path Delay Calculation – Slew Merging – Slack Calculation.

TEXT BOOKS / REFERENCES:

1. N.H.E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design*, Second Edition, Addison Wesley, 1993.
2. J.M. Rabaey, *Digital Integrated Circuits a Design Perspective*, Second Edition, Prentice Hall India, 2003.
3. J. Bhasker and R. Chadha, *Static Timing Analysis for Nanometer Designs: A Practical Approach*, Springer, 2009.
4. W.J. Dally and J.W. Poulton, *Digital Systems Engineering*, Cambridge University Press, 2008.
5. P.K. Lala, *Principles of Modern Digital Design*, John Wiley and Sons Ltd, 2007.

VL616 **LOW POWER VLSI CIRCUITS** **3-0-0-3**

Importance of Low Power Consumption – Design for Low Power – Deep Submicron and Nanometer MOS Transistors and Models – Sources of Static and Dynamic Power Consumption in MOS Devices – New Device Technologies for Reducing Leakage Current – Basics of Power and Energy – Power Optimization during Design Cycle – Architecture – Algorithm and System Levels – Power Optimization of Interconnects and Clocks – Dynamic Voltage Scaling – Clock Distribution – Power Optimization in Memories – Power in Cell Arrays – Power for Read and Write Accesses – Low Power Memory Technologies – Standby Power Optimization of Circuits and Systems – Power Optimization of Circuits and Systems during Operation – Low Power Design Methodologies and Flows – Power Characterization and Modeling – Low Power Clock – Data and Power Gating – Power Integrity.

TEXT BOOKS / REFERENCES:

1. J.M. Rabaey, *Low Power Design Essentials*, Springer, 2009.
2. C. Piguet, *Low-Power CMOS Circuits: Technology, Logic Design and CAD Tools*, CRC Press, Taylor and Francis, 2006.
3. R. Chadha and J. Bhaskar, *An ASIC Low Power Primer, Analysis, Techniques and Specification*, Springer, 2013.
4. D. Flynn, R. Aitken, A. Gibbons and K. Shi, *Low power Methodology Manual for System on Chip*, Springer, 2007.

VL617 **TESTING OF VLSI CIRCUITS** **3-0-0-3**

Introduction – Fault Modeling – Logic and Fault Simulation – Algorithms for True-value Simulation and Fault Simulation – Testability Measures – ATPG Fundamentals – Combinational Circuit Test Generation – Redundancy Identification – ATPG for Roth's D-algorithm – PODEM – Sequential Circuit Test Generation – Time Frame Expansion and Implementation – Introduction to Memory Test and Delay Test – DFT Fundamentals – Mux-D Scan Architectures – Level-sensitive Scan Design – Random Access Scan Technique – Introduction to BIST and Boundary Scan Architecture.

TEXT BOOKS / REFERENCES:

1. V.D. Agrawal and M.L. Bushnell, *Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits*, Springer, 2000.
2. P.K. Lala, *An Introduction to Logic Circuit Testing*, Morgan Claypool Publishers, 2009.
3. M. Abramovici, M.A. Breuer and A.D. Friedman, *Digital Systems Testing and Testable Design*, IEEE Press, 1994.

VL618 **SEMINAR** **0-0-2-2**

The students in consultation with the faculty advisors have to select a topic related to VLSI design and present it. A detailed report has to be submitted.

VL619 **VLSI DESIGN LAB II** **0-0-2-2**

Advanced Design and Verification Tools – Design Projects.

TEXT BOOKS / REFERENCES:
Laboratory Manuals

EN 600 **TECHNICAL WRITING**

Technical terms – Definitions – extended definitions – grammar checks – error detection – punctuation – spelling and number rules – tone and style – pre-writing techniques – Online and offline library resources – citing references – plagiarism – Graphical representation – documentation styles – instruction manuals – information brochures – research papers – proposals – reports (dissertation, project reports etc.) – Oral presentations.

TEXTBOOKS / REFERENCES:

1. H.L. Hirsch, *Essential Communication Strategies for Scientists, Engineers and Technology Professionals*, Second Edition, New York: IEEE press, 2002.
2. P.V. Anderson, *Technical Communication: A Reader-Centred Approach,* Sixth Edition, Cengage Learning India Pvt. Ltd., New Delhi, 2008, (Reprint 2010).
3. W.Jr. Strunk, and E.B. White, *The Elements of Style*, New York. Alliyan & Bacon, 1999.

VL701 **DIGITAL SIGNAL PROCESSING** **3-0-0-3**

Review of Signals and Systems – Review of Matrix Algebra – Vector Spaces – Linear Space Independence – Basis – Inner Product – Orthogonality – General Linear Transformation – Periodicity – Sampling of Continuous Signals – Discrete Frequency – Reconstruction and Aliasing – Fourier Transforms – Discrete Fourier Series for Periodic Sequences – DTFT – Discrete Fourier Transform and Properties – Circular Convolution – Fast Fourier Transform (FFT) – DFT – Relationship of DFT and other Transforms – Linear Filtering – Filter Design – FIR Filters – Design using Windows – Butterworth Filter Design – IIR Filters – Impulse Invariant and Bilinear Transformation Techniques – Filter Structures – Direct Form I – Direct Form II – Cascade and Parallel Structures – Introduction to Programmable DSPs – DSP Arithmetic – Fixed-point – Floating-point Representations – Introduction to Multi-rate Signal Processing – Basic Signal Processing Architectures – Modified Harvard – VLIW – MAC – Memories – Pipelining – Addressing Modes.

TEXT BOOKS/REFERENCES:

1. J.G. Proakis and D.G. Manolakis, *Digital Signal Processing, Principles, Algorithms and Applications*, Fourth Edition, Pearson Education, 2007.
2. B. Venkataramani and M. Baskar, *Digital Signal Processors, Architecture, Programming and Applications*, Tata McGraw-Hill, 2002, (Reprint 2008).
3. S.K. Mitra, *Digital Signal Processing*, Third Edition, Tata McGraw-Hill, 2006.

4. G. Strang, *Introduction to Linear Algebra*, Fourth Edition, Wellesley-Cambridge Press, 2009.
5. TI DSP Processors User Manual.

VL702 EMBEDDED SYSTEMS 3-0-0-3

Microcontroller Fundamentals – ARM-ASM Programming and basics of C – I/O Interfacing (LED and Switch) – Microcontroller Ports – Design and Development Process Architecture – Micro-architecture – Design – Implementation – Verification and Validation – Development Tools – Block Diagrams – Flowcharts – Call Graphs – Dataflow Graphs – Finite State Machines – Parallel Interface – GPIO – Serial Interface – UART – PLL Programming – Timer – Fixed Point Software – Structs – Stacks and Recursion using ASM Programming – Device Driver – Interfacing with a Hitachi HD XXX Display – I/O Synchronization – Interrupts – DAC – Music Synthesis and Music Playback – ADC – Real-world Interfacing and Data Acquisition – Applications using ADC, DAC, Interrupts, UART, Display Device Driver.

TEXT BOOKS/REFERENCES:

1. J. Valvano, *Embedded Systems: Introduction to ARM® Cortex™-M Microcontrollers*, Volume 1, Fourth Edition, Create Space Independent Publishing Platform, 2012.
2. A.S. Berger, *Embedded System Design*, CRC Press, 2001, (Reprint 2002).
3. D.E. Simon, *An Embedded Software Primer*, Pearson Education, 2001.
4. S. Heath, *Embedded Systems Design*, Second Edition, Newnes, 2002.

VL703 CMOS RF SYSTEM DESIGN 3-0-0-3

Introduction to Wireless Principles – Passive RLC Networks – Characteristics of Passive IC Components – Review of MOS Device Principles – Cut-off Frequency for CMOS based Circuits – Smith Chart and Scattering Parameters – Bandwidth Estimation Techniques – Diodes and Bipolar Transistors in CMOS Technology – Biasing Techniques – Noise Classification – Two Port Noise Calculations – Low Noise Amplifier Design – Transceiver Architecture – Dynamic Range – Stability Circles – Chip Design Examples.

TEXT BOOKS/REFERENCES:

1. T.H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*, Second Edition, Cambridge University Press, 2009.
2. B. Leung, *VLSI for Wireless Communication*, Second Edition, Pearson Education, 2007.
3. I. Hickman, *Practical RF Handbook*, Fourth Edition, Elsevier, 2007.
4. D.M. Dobkin, *RF Engineering for Wireless Networks*, Elsevier, 2005.

VL704 NANO ELECTRONICS 3-0-0-3

Introduction to Nano electronics – Quantum Mechanics of Electrons: General Postulates of Quantum Mechanics – Time Dependent Schrodinger's Equation – Probabilistic Current Density – Spin and Angular Momentum – Heterojunctions – Confined Electrons: Quantum Wells – Wires and Dots – Graphene – Carbon Nanotubes – Single Electron Phenomena – Quantum Blockade and SET – Nanowires – Ballistic and Spin Transport – Spin-electronics – Nano

Transistors: HEMT – FinFETs and other Advanced FETs – Technology for Nanostructures: MOCVD – MBE.

TEXT BOOKS / REFERENCES:

1. S. Datta, *Lessons from Nanoscience: A Lecture Notes Series: A New Perspective on Transport*, Volume 1, World Scientific, 2012.
2. Y. Taur and T.H. Ning, *Fundamentals of Modern VLSI Devices*, Second Edition, Cambridge University Press, 2009.
3. S.M. Sze and K.K. Ng, *Physics of Semiconductor Devices*, Third Edition, John Wiley and Sons Inc., 2006.
4. M. Lundstorm and J. Guo, *Nanoscale Transistors: Device Physics, Modeling and Simulation*, Springer Verlag, 2006.
5. G.W. Hanson, *Fundamentals of Nanoelectronics*, Pearson Education, 2013.
6. V.V. Martin, V.A. Kochelap and M.A. Stroscio, *Quantum Heterostructures: Miscoelectronics and Optoelectronics*, Cambridge University Press, 1999.

VL705 VLSI SIGNAL CONDITIONING 3-0-0-3

Operational Trans-conductance Amplifier basic Considerations – Application Requirements for OTAs used in Filters – The Case for Fully Differential Circuits – Transistor Models – G_m/I_D-based Design – Single-stage OTAs – Basic Differential Pair – Telescopic Architecture – Folded Cascode Architecture – Two-stage OTA – Gain Boosting – Common-mode Feedback Implementation– G_m-C Biquad – Trans-conductor Implementation – NAUTA Cell – Source Follower based Filter – Parameter Tuning – Q-tuning – VCF-tuning – Discrete Frequency Tuning / Programming – Tuning G_m over a Wide Range – Switched Capacitor Filters – Parasitic Sensitive Configurations – Transient and Circuit Analysis – Frequency Response – Aliasing – Periodic AC Analysis – SC Integrators – Martin-Sedra Biquad – Low and High Q Biquads – Noise Analysis – Precision Analog Circuit Design – Precision Analog Circuit Techniques – Introduction – Applications.

TEXT BOOKS / REFERENCES:

1. R. Schauman, H. Xiao and M.V. Valkenburg, *Design of Analog Filters*, Second Edition, Oxford University Press, 2009.
2. T.C. Carusone, D.A. Johns and K.W. Martin, *Analog Integrated Circuit Design*, Second Edition, John Wiley Inc., 2012.
3. R. Gregorian and G.C. Temes, *Analog MOS Integrated Circuits for Signal Processing*, Wiley, 1986.

VL706 SYSTEM ON CHIP DESIGN 3-0-0-3

Comparison of Different Computing Methods – Fundamentals of FPGA Architectures – FPGA Placement and Routing – FPGA Configuration – HDL based Design of Combinational and Sequential Logic Modules – Tools for Design and Prototyping – Design of Advanced FPGA-based Systems with Soft-core Microprocessors – Interface to Hard-core Microprocessors –

Reconfigurable Computing Architectures – Applications of Reconfigurable Computing – High-level Compilation – Hardware/Software Partitioning.

TEXT BOOKS / REFERENCES:

1. S. Hauck and A. Dehon, *Reconfigurable Computing*, Morgan Kaufmann, 2008.
2. M. Gokhale and P. Graham, *Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays*, Springer, 2005.
3. C. Maxfield, *The Design Warrior's Guide to FPGAs*, Newnes, 2004.
4. W. Wolf, *FPGA based System Design*, Prentice Hall, 2004.
5. S. Kilts, *Advanced FPGA Design: Architecture, Implementation and Optimization*, Wiley, 2007.

VL707 VLSI ARCHITECTURES FOR MULTI-CORE AND HETEROGENEOUS COMPUTING 3-0-0-3

Review of Superscalar Processing and Pipelining – Instruction Level Parallelism – Branch Prediction and Speculation – Static and Dynamic Scheduling – Limits of ILP – Multi-issue and Multi-core Processors – Shared and Dedicated Bus Multiprocessor Architectures – VLSI Multiprocessor Interconnection Networks – Interaction between Heterogeneous Models – VLSI architecture – Introduction to Programming Models for Heterogeneous Computing – Communication Synchronization and Memory Hierarchy including Cache Design and Coherency in Single Chip Heterogeneous Computing – Heterogeneous Multi-processing on a Single Chip (System-on-Chip) – Network-on-Chip (NoC) – Interconnection and VLSI models for NoC – Power Optimization in Heterogeneous Computing – VLSI Models for Specialized and Domain Specific Heterogeneous Computing Architectures – Case Studies of VLSI Architectures for Multi-core Processors.

TEXT BOOKS / REFERENCES:

1. M. Moonen and F. Catthoor, *Algorithms and Parallel VLSI Architectures III*, Elsevier, 1995.
2. J. Dongarra and A.L. Lastovetsky, *High Performance Heterogeneous Computing*, Wiley Series, 2009.
3. K. Uchiyama, F. Arakawa, H. Kasahara, T. Nojiri, H. Noda, Y. Tawara, A. Idehara, K. Iwata, and H. Shikano, *Heterogeneous Multi-core Processor Technologies for Embedded Systems*, Springer, 2012.
4. J. L. Hennessy and D.A. Patterson, *Computer Architecture: A Quantitative Approach*, Fourth Edition, Morgan Kaufmann, 2011.

VL708 ANALOG SUB-SYSTEM DESIGN 3-0-0-3

Feedback of Op-amps – Noise – Ideal Sampling – Reconstruction – Amplifiers – Integrators – Introduction and Principles of ADCs and DACs – Performance Metrics of ADCs and DACs – Nyquist Rate DACs – Comparators Characterization – Two Stage Comparators – Open Loop Comparators – Analog Multiplier Design – Simple PLL – Charge Pump PLL – Applications of PLL – Nyquist Rate ADCs – Oversampling ADCs – Testing of ADCs.

TEXT BOOKS / REFERENCES:

1. J.R. Baker, *CMOS: Mixed–Signal Circuit Design*, Second Edition, Wiley-IEEE Press, 2009.
2. B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2000.
3. D.A. Johns and K. Martin, *Analog Integrated Circuit Design*, Second Edition, Wiley, 2011.
4. B. Razavi, *Principles of Data Conversion System Design*, IEEE Press, 1995.

VL709 VLSI SIGNAL PROCESSING 3-0-0-3

Introduction to Digital Signal Processing Systems – Iteration Bound – Pipelining and Parallel Processing – Retiming – Unfolding – Folding – Systolic Architecture Design – Scaling and Round off Noise – Programmable Digital Signal Processors – Computational Accuracy in DSP Implementations – Adaptive Filters-Kalman Filters.

TEXT BOOKS / REFERENCES:

1. K.K. Parhi, *VLSI Digital Signal Processing Systems, Design and Implementation*, Wiley, 1999.
2. B. Venkataramani, and M. Baskar, *Digital Signal Processors, Architecture, Programming and Applications*, Tata McGraw-Hill, 2002, (Reprint 2008).
3. A. Singh and S. Srinivasan, *Digital Signal Processing Implementations using DSP Microprocessors with examples from TMS320C54XX*, Thomson Learning, 2004.
4. S. Haykin, *Adaptive Filter Theory*, Prentice Hall, 1997.

VL710 HARDWARE SOFTWARE CO-DESIGN 3-0-0-3

Introduction to System Level Design – Models of Computation – Architectural Selection – Partitioning – Scheduling – Communication – Simulation – Synthesis and Verification – Implementation Case Studies – Performance Analysis and Optimization – Re-targetable Code Generation – FPGAs.

TEXT BOOKS / REFERENCES:

1. P.R. Schaumont, *A Practical Introduction to Hardware/Software Co-design*, Springer India, 2010.
2. J. Staunstrup and W. Wolf, *Hardware/Software Co-design: Principle and Practice*, Kluwer Academic Publishers, 1997.
3. G. De Micheli, *Readings in Hardware Software Co-design*, Morgan Kaufmann, Academic Press, 2002.
4. S.-J. Chen, K.-H. Lin, P.-A. Hsiung and Y.-H. Hu, *Hardware Software Co-Design of a Multimedia SOC Platform*, Springer, 2010.
5. J.V.D. Hurk and J.A.G. Jess, System *Level Hardware/Software Co-Design: An Industrial Approach*, Springer, 1998.

VL711 VLSI HARDWARE SECURITY AND TRUST 3-0-0-3

Integrated Circuits (IC) Trojans – Vulnerabilities in Combinational and Sequential Logic – Finite State Machines – Trojan Attacks – Detection and Isolation – Side-channel Attacks include Power Spectrum Analysis – EM Analysis – Timing Analysis – Fault Injection – FPGA Security Attacks such as Hardware Trojans in Bit Files – Physical Attacks on FPGA – Physical Design

Layers – Emerging Hardware Security Topics – Trusted Platform Modules (TPM) for Hardware – Physically Unclonable Functions (PUFs) – True Random Number Generators (TRNG) – RFID Tag – Hardware System Tampering – Tamper Resistant Hardware Design Techniques – Anti-Counterfeiting for Microelectronics Devices – Protection of Intellectual Property (IP) – Discussions on IC Reverse Engineering – Methods to Make Reverse Engineering Harder – Non-standard Cell Libraries – Reduction in Feature Sizes.

TEXT BOOKS / REFERENCES:

1. M. Tehranipoor and C. Wang, *Introduction to Hardware Security and Trust*, Springer, 2011.
2. J. Plusquellic, *Trojan Taxonomy*, University of New Mexico, http://www.ece.unm.edu/~jimp/HOST.
3. D. Agrawal, S. Baktir, D. Karakoyunlu, P. Rohatgi, and B. Sunar, *Trojan Detection using IC fingerprinting*, Symposium on Security and Privacy, 2007.
4. G. Edward Suh and S. Devadas, *Physical Unclonable Functions for Device Authentication and Secret Key Generation*, DAC-2007.
5. R. Torrance and D. James, *The state-of-the art in IC Reverse Engineering, Cryptographic Hardware and Embedded Systems* - CHES 2009 Lecture Notes in Computer Science Volume 5747, pp. 363-381, Springer, 2009.

VL712 RECONFIGURABLE COMPUTING 3-0-0-3

Introduction – Goals and Motivations – History – State-of-the-Art – Future Trends – Von-Neumann Architecture Versus Reconfigurable Computing (RC) – Commercial FPGA based RC – Custom Configurable Hardware based RC – Advanced Technologies in Field Programmable Logic Devices – Topics include General RC Concepts – Fine Grain and Coarse Grain RC Architectures – RC Design Tools – RC Metrics and Application – Case Studies in Signal/Image processing – Bio Informatics.

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1. S. Hauck and A. Dehon, *Reconfigurable Computing: The Theory and Practice of FPGA-Based Computing*, Morgan Kaufmann, 2007.
2. M. Gokhale and P. Graham, *Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays*, Springer, 2005.
3. C. Bobda, *Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications*, Springer, 2007.
4. R. Cofer and B. Harding, *Rapid System Prototyping with FPGAs: Accelerating the Design Process*, Newnes, 2005.

VL713 ELECTRONIC SYSTEM LEVEL DESIGN 3-0-0-3

Introduction to Electronic System Level Design – ESLD Flows and Methodologies – Architecture Exploration – Hardware-Software Partitioning – Models for System Level Design – Functional Simulation – HW-SW Co-Verification – Verification Plan Creation – Random Stimuli based Test Bench Writing – Test Coverage – Open Source Tools – Bluespec and

Accellera – System-C for Design – System Verilog and E for Verification – Project based ESLD Design and Verification.

TEXT BOOKS / REFERENCES:

1. S. Rigo, R. Azevedo and L. Santos, *Electronic System Level Design – An Open-Source Approach*, Springer, 2011.
2. B. Bailey and G. Martin, *ESL Models and their Application for Electronic System Level Design and Verification in Practice*, Springer, 2010.
3. M. Burton and A. Morawiec, *Platform based Design at the Electronic System Level - Industry Perspectives and Experiences*, Springer, 2006.
4. R. Zurawaski, *Embedded Systems Design and Verification*, CRC Press, 2009.
5. C. Grimm, *Languages for System Specification*, Springer, 2004.

VL714 MONOLITHIC MICROWAVE INTEGRATED CIRCUITS 3-0-0-3

Planar Circuit Fundamentals – Discontinuities – Transitions – Thin-film Resistors – Metal – Insulator – Metal Overlay Capacitors – Inter Digitated Capacitors – Spiral Inductors – Fabrication Technologies – Measurements – Test Systems – Dielectric – Magnetic and Substrate Materials – Multi-band Multi-standard LNA with CPW Transmission Line Inductor – Design of Low Noise Amplifiers using Flow Graphs Optimization – Simulated Annealing Technique – Design and Modeling of 2.4 GHz and 3.5 GHz MMIC Power Amplifier – RF and Microwave Test of MMICs.

TEXT BOOKS / REFERENCES:

1. A. Marzuki, A.I.A. Rahim and M. Loulou, *Advances in Monolithic Microwave Integrated Circuits for Wireless Systems: Modeling and Design Technologies*, IGI-Global Press, 2011.
2. Y. Konishi, *Microwave Integrated Circuits*, Marcel Dekker Inc., 2009.
3. R.K. Hoffmann, *Handbook of Microwave Integrated Circuits*, Artech House, 1987.

VL715 DESIGN FOR TEST 3-0-0-3

Design for Testability – Testability Trade-offs and Techniques – Scan Architectures and Testing – Controllability and Observability – Testing of DRAM and SRAMs – RAM Fault Modeling – Non-volatile Memory Modeling – Electrical Testing – Pseudo Random Testing – Memory BIST – Specific BIST Architectures – CSBL – BEST – RTS – LOCST – STUMPS – CBIST – CEBS – RTD – SST – CATS – CSTP – BILBO – Analog and Mixed Signal Test – Model based Testing – Analog ATPG using Signal Flow Graphs – Transition Faults – I_{DDQ} Testing Methods – DFT Fundamentals – Digital DFT and Scan Design – At-speed Testing – Boundary Scan Architecture – JTAG Standards – Boundary Scan Instructions.

TEXT BOOKS / REFERENCES:

1. V.D. Agrawal and M.L. Bushnell, *Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits*, Springer, 2000.
2. M. Abramovici, M. A. Breuer and A. D. Friedman, *Digital Systems Testing and Testable Design*, IEEE Press, 1994.
3. A.L. Crouch, *Design for Test for Digital ICs and Embedded Core Systems*, Prentice Hall, 1999.

VL716 **NETWORK ON CHIP** **3-0-0-3**

Introduction to NoC – NoC in SoC Context – OSI layer Roles in NoC – Benefits and Challenges in adapting NoCs – NoC Modeling – Topology Exploration – Traffic Modeling – Topology Modeling – Communication Architecture – Switching Technique – Packet Routing – QoS – Congestion and Flow Control – Router Design – Interconnect Techniques – Reduced Swing Circuits – Current-mode Transmission Techniques – CMOS Repeater Design – Driving Interconnects for Optimum Speed and Power – Short Channel Model of CMOS Repeater – Transient Analysis of an RC Loaded CMOS Repeater – CMOS Repeater Insertion – Delay and Power of a Repeater Chain Driving an RC Load – Crosstalk – Circuit Level Modeling of Crosstalk – Power and Energy Savings in NOCs – NOC Based System Integration – NOC Interface Design – Clock Distribution.

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1. K. Tatas, K. Siozios, D. Soudris and A. Jantsch, *Designing 2D and 3D Network on chip Architecture*, Springer, 2013.
2. G. De Micheli and L. Benini, *Network on Chip: Technology &Tools*, Morgan Kaufmann Publisher, 2006.
3. F. Moll and M. Roca, *Interconnection Noise in VLSI Circuits*, Kluwer Academic Publishers, 2003.
4. A. Jantsch and H. Tenhunen (Eds.), *Network on Chip*, Kluwer Academic Publishers, 2003.
5. N. Chrysostomos and N. Vijayakrishnan, *Network on Chip Architecture: A Holistic Design exploration*, Lecture Notes in Electrical Engineering, Springer, 2009.
6. W.J. Dally and B. Towles, *Principles and Practices of Interconnection Networks*, Morgan Kaufmann Publishers, 2004.

VL717 **OPTIMIZATION TECHNIQUES FOR VLSI DESIGN** **3-0-0-3**

Statistical Modeling – Modeling Sources of Variations – Monte Carlo Techniques – Process Variation Modeling – Pelgrom's Model – Response Surface Methodology – Delay Modeling – Interconnect Delay Models – Statistical Performance – Power and Yield Analysis – Statistical Timing Analysis – Parameter Space Techniques – High Level Statistical Analysis – Approximation and Fitting – Monomial fitting – Max-monomial Fitting – Polynomial Fitting – Genetic Algorithm – Introduction – GA Technology – Steady State Algorithm – Fitness Scaling – Inversion – GA for VLSI Design – GA Routing Procedures and Power Estimation – Global Routing – FPGA Technology Mapping – Circuit Generation – Power Estimation – Application of GA – Fitness Function – Data-fitting Methods – Regression Analysis – Analysis of Variance – Goodness of Fit – Probability and Random Processes – Discrete and Continuous Distribution – Stochastic Processes – Time Series Models – Modeling and Simulation – Concepts – Discrete-event simulation – Event scheduling / Time advance algorithms – Verification and Validation of Simulation Models.

TEXT BOOKS / REFERENCES:

1. A. Srivatava, D. Sylvester and D. Blauw, *Statistical Analysis and Optimization for VLSI Timing and Power*, Springer, 2008.

2. P. Mazumder, and E. Mrudnick, *Genetic Algorithm for VLSI Design Layout and Test Automation*, Prentice Hall India, 1998.
3. Z. Navabi, *VHDL: Analysis and Modeling of Digital Systems*, Second Edition, McGraw Hill, 1998.
4. J. Banks, J.S. Carson and B. Nelson, *Discrete-Event System Simulation*, Fifth Edition, Prentice Hall India, 2009.

VL718 WAVELETS AND APPLICATIONS 3-0-0-3

Review of Fourier Theory – Heisenberg's Uncertainty Principle – Continuous Wavelet Transform (CWT) – Properties – Discrete Wavelet Transform (DWT) – Time-frequency Tiling – Short Time Fourier Transform – Wavelet and MRA – Vector Spaces – Scaling and Wavelet Functions – Filter Banks – Legendre Polynomials – Recurrence Formula – Laplace's Integral Formula – Design of Orthogonal Wavelet Systems – Bi-orthogonal Wavelet – Introduction to Lifting Scheme – Dealing with Signal Boundaries – Multi Wavelet – Frequency Domain Approach – Design of Wavelet – Wavelet in Image Processing – Biomedical Applications – Data Compression – EZW Algorithm – De-noising – Edge Detection – Object Isolation – Audio Coding – Communication Applications – Channel Coding – Speckle Removal – Image Fusion.

TEXT BOOKS / REFERENCES:

1. K.P. Soman and K.I. Ramachandran, *Insight into Wavelets from Theory to Practice*, Prentice Hall, 2004.
2. G. Strang and T. Q. Nguyen, *Wavelets and Filter Banks*, Wellesley Cambridge Press, 1998.
3. B.S. Grewal, *Higher Engineering Mathematics*, Khanna Publisher, 2000.
4. R.M. Rao and A.S. Bopardikar, *Wavelet Transforms - Introduction to Theory and Applications*, Pearson Education, 1999.
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VL719 SEMICONDUCTOR MEMORY DESIGN 3-0-0-3

Random Access Memory Technologies – SRAM Cell Structures – MOS SRAM Architecture – MOS SRAM Cell and Circuit Operation – Advanced SRAM Architectures and Technologies – Application Specific SRAMs – CMOS – DRAM – DRAM Cell Theory – Cell Structures – Soft Error Failure in DRAM – EEPROM Technology – Architecture – Non-volatile SRAM – Flash Memories – Advanced Flash Memory Architecture – RAM Fault Modeling – Volatile and Non-volatile Memory Testing Methods – RAM Fault Modeling – BIST Techniques for Memory – General Reliability Issues – RAM Failure Modes and Mechanism – Non-volatile Memory Reliability – Reliability Modeling and Failure Rate Prediction – Design for Reliability– Reliability Test Structures – Radiation Effects – Single Event Phenomenon (SEP) – FRAMs – GaAs RAMs – Magneto Resistive RAMs (MRAMs) – Experimental Memory Devices – Memory Hybrids and MCMs (2D) – Memory Stacks and MCMs (3D) – Memory MCM Testing and Reliability Issues – Memory Cards – High Density Memory Packaging.

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1. A.K. Sharma, *Semiconductor Memories: Technology, Testing, and Reliability*, Wiley, 2013.

2. S.K. Kurinec and K. Iniewski, *Nanoscale Semiconductor Memories: Technology and Applications*, CRC press, 2013.
3. K. Ishibashi and K. Osada, *Low Power and Reliable SRAM Memory Cell and Array Design*, Springer, 2011.

VL720 STATIC TIMING ANALYSIS 3-0-0-3

Static Timing Analysis – Concepts – Capacitance and Transition Violations – Temperature, Voltage and Process – Constraining I/O Interface Paths – Cell Delay – Net Delay – Interconnect Delay – Crosstalk and Noise – Crosstalk Glitch Analysis – Crosstalk Delay Analysis – Setup-Hold Analysis – Timing Verification – Setup-Hold Timing Checks – Synchronization – Synchronization Failure – Probability of Entering a Meta-stable State – Probability of Staying in the Meta-stable State – Multi-cycle Paths – False Paths – Timing Across Clock Domains – Clock Network Optimization – Clock Skew – Scheduling – Clock Distribution Problem – Off-chip Clock Distribution – Clock Trimming – On-chip Clock Distribution and Tree – Reducing Jitter – Pre-layout Clock Specification – Post-layout Clock Specification – Parallel Timing Optimization – Circuit Partitioning for Independent Timing Regions – Post-silicon Timing Validation – Introduction – Sources of Post-silicon Timing Failure – Post-silicon Tuning – On-chip Variations – Time Borrowing – Clock Gating Checks – Sign-off Methodology – Statistical Static Timing analysis.

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1. J. Bhasker and R. Chadha, *Static Timing Analysis for Nanometer Designs: A Practical Approach*, Springer, 2009.
2. C. J. Alpert, D.P. Mehta and S.S. Sapatnekar, *Handbook of Algorithms for Physical Design Automation*, CRC Press, 2009.
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4. E. Bogatin, *Signal and Power Integrity*, Second Edition, Pearson Education, 2010.

VL721 SYNTHESIS AND VERIFICATION OF VLSI LOGIC DESIGN 3-0-0-3

Logic Design – Logic Synthesis – Logic Optimization – Two Level Logic Optimization – Multi Level Logic Optimization – Optimization – Optimization for Low Power – Engineering Change In Logic Synthesis for Arithmetic Circuit – FSM Synthesis – FSM optimization – Hierarchical logic synthesis – Multi Level Logic Synthesis – Logic Verification – Formal Method – Binary Decision Diagram (BDD) – Satisfiable Problem and Solver – Model Checking – Bounded Model Checking – Combinational Equivalence Checking – Sequential Equivalence Checking – Assertion based Formal Verification – Logic Design Debug and Analysis.

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1. G. De Micheli, *Synthesis and Optimization of Digital Circuits*, Mc Graw-Hill series in Electrical and Computer Engineering: Electronics and VLSI Circuits, 2003.
2. T. Sasa, *Logic Synthesis and Optimization Series*, The Springer International Series in Engineering and Computer Science, Vol. 212, 1993.
3. M. Fujita, I. Ghosh, and M. Prasad, *Verification Techniques for System-Level Design (System on Silicon)*, Morgan Kaufmann, 2007.

4. G.D. Hachtel and F. Somenzi, *Logic Synthesis and Verification Algorithms*, Kluwer Academic Publishers, 2002.
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VL722 OPTOELECTRONIC DEVICES 3-0-0-3

Energy Levels and Bands in Solids – Optoelectronic Materials – Epitaxial Growth Technology – Carrier Generation and Recombination in Active Regions – Spontaneous and Stimulated Transitions – Threshold and Steady State Gain in Lasers – Threshold Current and Power – Rate equations – Steady State Solutions – Differential Analysis – Large Scale Analysis – Mode Locking – Frequency Chirping – Characterization on Laser Diode – Mirrors and Resonators – Three and Four Mirror Laser Cavities – Periodic Structures – Perturbation Theory – DBF and DFB lasers – Vertical Cavity Surface Emitting Lasers – Modal Excitation – Optical bi-Stability – Photonic Detectors – Photonic Integrated Circuits – Optical Switches – Optical Interconnectors – Optical Waveguides – Semiconductor Optical Amplifiers – Photonic Multiplexers – De-multiplexers and Routers – Optoelectronics for Coherent Optical Communication – Optical Computing.

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1. L.A. Coldren, S.W. Corzine and M.L. Masanovic, *Diode Lasers and Photonic Integrated Circuits*, Second Edition, Wiley, 2012.
2. B.E.A. Saleh and M.C.Teich, *Fundamentals of Photonics*, Wiley, 2007.
3. S.O. Kasap, *Optoelectronics and Photonics: Principles and Practices*, Second Edition, Prentice Hall, 2012.